IN THE CLAIMS

1. (Currently Amended) A memory module, comprising:

a support;

a plurality of leads extending from the support;

a command link coupled to at least one of the plurality of leads;

a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and

at least one memory device contained on the support and coupled to the command link, wherein the ~~at least one~~ memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a bottom electrode;

a top electrode;

a dielectric layer interposed between the bottom electrode and the top electrode; and

at least one metal oxynitride barrier layer, wherein each metal oxynitride barrier layer is interposed between the dielectric layer and an electrode selected from the group consisting of the bottom electrode and the top electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

2. (Currently Amended) The memory module of claim 1, wherein the ~~at least one~~ metal oxynitride barrier layer comprises MO_xN_y, wherein M is a metal selected from the group consisting of: chromium, cobalt, hafnium, iridium, molybdenum, niobium, osmium, rhenium, rhodium, ruthenium, tantalum, titanium, tungsten, vanadium and zirconium.

3. (Original) The memory module of claim 2, wherein x ranges from approximately 0.05 to approximately one-half the maximum valence value of the metal M minus 0.05 and y ranges from approximately 0.1 to approximately the maximum valence value of the metal M minus 0.1.

4. (Original) The memory module of claim 2, wherein M is a metal selected from the group consisting of chromium, hafnium, molybdenum and tungsten, and wherein x ranges from approximately 0.05 to approximately 2.95 and y ranges from approximately 0.1 to approximately 5.9.

5. (Currently Amended) The memory module of claim 1, wherein the ~~at least one~~ metal oxynitride barrier layer comprises a tungsten oxynitride having a composition of the form WO_xN_y, wherein x ranges from approximately 0.05 to approximately 2.95 and y ranges from approximately 0.1 to approximately 5.9.

6. (Currently Amended) The memory module of claim 1, wherein at least one electrode selected from the group consisting of the bottom electrode and the top electrode comprises a metal nitride.

7. (Currently Amended) The memory module of claim 1, wherein at least one electrode selected from the group consisting of the bottom electrode and the top electrode comprises tungsten nitride.

8. (Original) The memory module of claim 1, wherein dielectric layer includes a metal oxide selected from the group consisting of $Ba_zSr_{(1-z)}TiO_3$, (where $0 < z < 1$), $BaTiO_3$, $SrTiO_3$, $PbTiO_3$, $Pb(Zr,Ti)O_3$, $(Pb,La)(Zr,Ti)O_3$, $(Pb,La)TiO_3$, Ta_2O_5, KNO_3, Al_2O_3 and $LiNbO_3$.

9. (Currently Amended) The memory module of claim 1, wherein the ~~metal oxide~~ dielectric layer comprises tantalum oxide.

10. (Currently Amended) A memory module, comprising:

a support;

a plurality of leads extending from the support;

a command link coupled to at least one of the plurality of leads;

a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and

at least one memory device contained on the support and coupled to the command link, wherein the ~~at least one~~ memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a bottom electrode;

a top electrode;

a dielectric layer interposed between the bottom electrode and the top electrode; and

at least one tungsten oxynitride barrier layer, wherein each tungsten oxynitride barrier layer is interposed between the dielectric layer and an electrode selected from the group consisting of the bottom electrode and the top electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

11. (Currently Amended) The memory module of claim 10, wherein the ~~at least one~~ tungsten oxynitride barrier layer has a composition of the form WO_xN_y, wherein x ranges from approximately 0.05 to approximately 2.95 and y ranges from approximately 0.1 to approximately 5.9.

12. (Currently Amended) The memory module of claim 10, wherein at least one electrode selected from the group consisting of the bottom electrode and the top electrode comprises a metal nitride.

13. (Currently Amended) The memory module of claim 10, wherein at least one electrode selected from the group consisting of the bottom electrode and the top electrode comprises tungsten nitride.

14. (Canceled)

15. (Currently Amended) A memory module, comprising:

a support;

a plurality of leads extending from the support;

a command link coupled to at least one of the plurality of leads;

a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and

at least one memory device contained on the support and coupled to the command link, wherein the ~~at least one~~ memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a bottom electrode;

a top electrode;

a metal oxide dielectric layer interposed between the bottom electrode and the top electrode; and

at least one tungsten oxynitride barrier layer, wherein each tungsten oxynitride barrier layer is interposed between the metal oxide dielectric layer and an electrode selected from the group consisting of the bottom electrode and the top electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit wherein at least one electrode selected from the group consisting of the bottom electrode of the capacitor and the top electrode of the capacitor comprises tungsten nitride.

16. (Original) The memory module of claim 15, wherein the metal oxide layer comprises tantalum oxide.

17. (Original) The memory module of claim 15, wherein the bottom and top electrodes comprise tungsten nitride.

18. (Currently Amended) A module comprising:

a support;

a plurality of leads extending from the support;

a command link coupled to at least one of the plurality of leads;

a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and

at least one memory device contained on the support and coupled to the command link, wherein the ~~at least one~~ memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a bottom electrode having a bottom electrode metal component;

a top electrode having a top electrode metal component;

a dielectric layer interposed between the bottom electrode and the top electrode; and

at least one metal oxynitride barrier layer having a barrier metal component, wherein the barrier metal component is different from the bottom electrode metal component or wherein the barrier metal component is different from the top electrode metal component, wherein the ~~at least one~~ metal oxynitride barrier layer is interposed between the dielectric layer and the bottom electrode or wherein the ~~at least one~~ metal oxynitride layer is interposed between the dielectric layer and the top electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

19. (Original) The module of claim 18, wherein the metal oxynitride barrier layer comprises MOxNy, wherein M is a metal selected from the group consisting of: chromium, cobalt, hafnium, iridium, molybdenum, niobium, osmium, rhenium, rhodium, ruthenium, tantalum, titanium, tungsten, vanadium and zirconium.

20. (Original) The module of claim 19, wherein x ranges from approximately 0.05 to approximately one-half the maximum valence value of the metal M minus 0.05 and y ranges from approximately 0.1 to approximately the maximum valence value of the metal M minus 0.1.

21. (Original) The module of claim 19, wherein M is a metal selected from the group consisting of chromium, hafnium, molybdenum and tungsten, and wherein x ranges from approximately 0.05 to approximately 2.95 and y ranges from approximately 0.1 to approximately 5.9.

22. (Currently Amended) The module of claim 18, wherein the ~~at least one~~ metal oxynitride barrier layer comprises a tungsten oxynitride having a composition of the form WOxNy, wherein x ranges from approximately 0.05 to approximately 2.95 and y ranges from approximately 0.1 to approximately 5.9.

23. (Original) The module of claim 18, wherein one of the top and bottom electrodes comprises a metal nitride.

24. (Original) The module of claim 18, wherein one of the top and bottom electrodes comprises tungsten nitride.

25. (Original) The module of claim 18, wherein the dielectric layer comprises a metal oxide dielectric material selected from the group consisting of $BazSr_{(1-z)}TiO_3$, (where $0 < z < 1$), $BaTiO_3$, $SrTiO_3$, $PbTiO_3$, $Pb(Zr,Ti)O_3$, $(Pb,La)(Zr,Ti)O_3$, $(Pb,La)TiO_3$, Ta_2O_5, KNO_3, Al_2O_3 and $LiNbO_3$.

26. (Original) The module of claim 18, wherein the dielectric layer comprises tantalum oxide.

27. (Currently Amended) A module comprising:

a support;

a plurality of leads extending from the support;

a command link coupled to at least one of the plurality of leads;

a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and

at least one memory device contained on the support and coupled to the command link, wherein the ~~at least one~~ memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a bottom electrode having a bottom electrode metal component;

a top electrode having a top electrode metal component;

a dielectric layer interposed between the bottom electrode and the top electrode; and

at least one tungsten oxynitride barrier layer having a barrier metal component, wherein the barrier metal component is different from the bottom electrode metal component or wherein the barrier metal component is different from the top electrode metal component, wherein the ~~at least one~~ tungsten oxynitride barrier layer is interposed between the dielectric layer and the bottom electrode or wherein the ~~at least one~~ tungsten oxynitride layer is interposed between the dielectric layer and the top electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

28. (Original) The module of claim 27, wherein the tungsten oxynitride barrier layer has a composition of the form WOxNy, wherein x ranges from approximately 0.05 to approximately 2.95 and y ranges from approximately 0.1 to approximately 5.9.

29. (Original) The module of claim 27, wherein one of the top and bottom electrodes comprises a metal nitride.

30. (Currently Amended) A module comprising:

a support;

a plurality of leads extending from the support;

a command link coupled to at least one of the plurality of leads;

a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and

at least one memory device contained on the support and coupled to the command link, wherein the ~~at least one~~ memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a bottom electrode having a bottom electrode metal component;

a top electrode having a top electrode metal component;

a metal oxide dielectric layer interposed between the bottom electrode and the top electrode; and

at least one tungsten oxynitride barrier layer having a barrier metal component, wherein the barrier metal component is different from the bottom electrode metal component or wherein the barrier metal component is different from the top electrode metal component, wherein the ~~at least one~~ tungsten oxynitride barrier layer is interposed between the metal oxide dielectric layer and the bottom electrode or wherein the ~~at least one~~ tungsten oxynitride layer is interposed between the metal oxide dielectric layer and the top electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit;

wherein one of the bottom and top electrodes comprises a metal nitride.

31. (Currently Amended) The module of claim 30, wherein the ~~at least one~~ tungsten oxynitride barrier layer has a composition of the form WOxNy, wherein x ranges from approximately 0.05 to approximately 2.95 and y ranges from approximately 0.1 to approximately 5.9.

32. (Original) The module of claim 30, wherein the metal oxide dielectric layer comprises tantalum oxide.

33. (Original) The module of claim 30, wherein the bottom and top electrodes comprise tungsten nitride.

34. (Currently Amended) A module comprising:

a support;

a plurality of leads extending from the support;

a command link coupled to at least one of the plurality of leads;

a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and

at least one memory device contained on the support and coupled to the command link, wherein the ~~at least one~~ memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a top electrode having a top electrode metal component and a bottom electrode having a bottom electrode metal component;

a dielectric layer comprising at least one metal oxide separating the bottom and top electrodes;

at least one metal oxynitride barrier layer arranged between the dielectric layer and one of the top and bottom electrodes, wherein the ~~at least one~~ metal oxynitride barrier layer having a barrier metal component, wherein the barrier metal component is different from the bottom electrode metal component or wherein the barrier metal component is different from the top electrode metal component;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

35. (Original) The module of claim 34, wherein the top electrode comprises tungsten nitride.